METHOD AND APPARATUS FOR DIGITAL FREQUENCY SYNTHESIS

ABSTRACT OF THE DISCLOSURE

A digital frequency synthesizer includes one or more reference clocks (104, 1316, 1502A, 1504A, 1506A) optionally coupled through one or more pulse width reducers (106) to one or more main delay lines (108, 702, 1502B, 1504B, 1506B) that include a plurality of output taps (108B-108I, 702B-702E). During at least certain periods of the reference clock (104) a plurality of the output taps are coupled to a common output (130, 1312, 1508), thereby producing an output signal that has a frequency that exceeds a frequency of the one or more reference clocks. The coupling is preferably accomplished by transmission gates (114, 128, 720-724, 1420-1434) that are switched by gating pulses that are received from decoders (148, 150, 1418) via gating signal delay lines (134-146, 704-718, 1404-1416).